UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,051,239 B2
APPLICATION NO. : 10/034717
DATED : May 23, 2006
INVENTOR(S) : Timothe Litt

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

The title page should be deleted and substitute therefore the attached title page.

Sheet 1 of 5 – Drawings
Fig. 1, replace with the following figure:

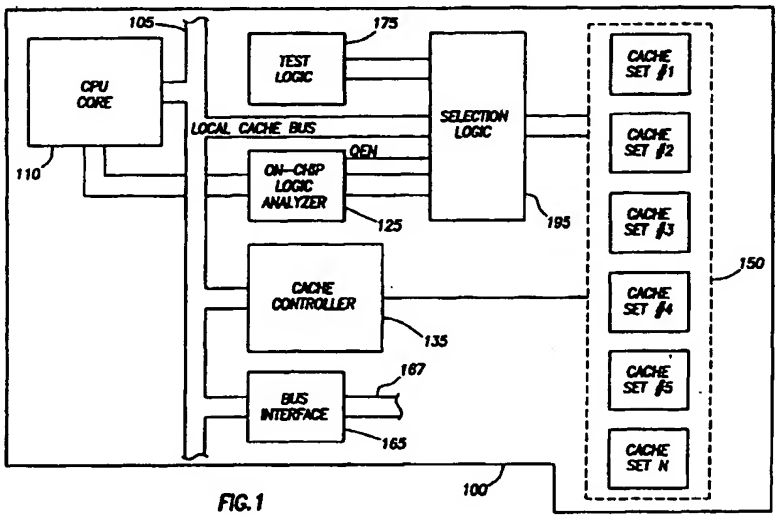

FIG. 1

Sheet 2 of 5 – Drawings
Fig. 2, replace with the following figure:

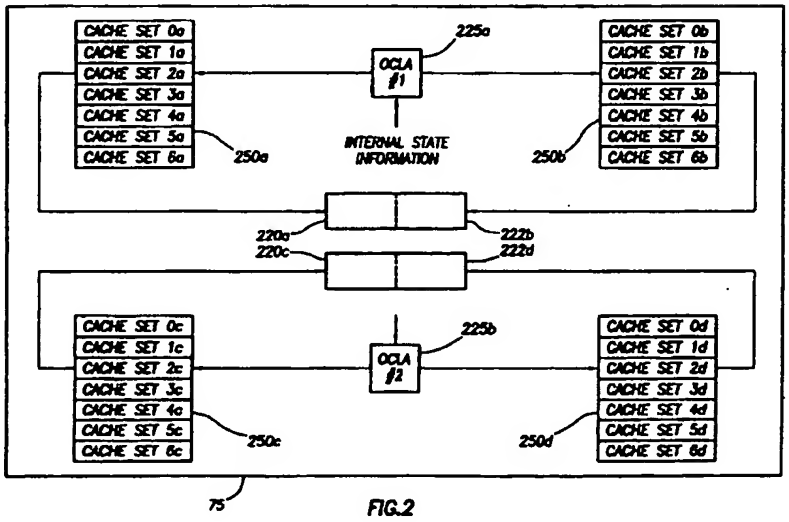

FIG. 2

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,051,239 B2
APPLICATION NO. : 10/034717
DATED : May 23, 2006
INVENTOR(S) : Timothe Litt

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Sheet 3 of 5 – Drawings
Fig. 3A, replace with the following figure:

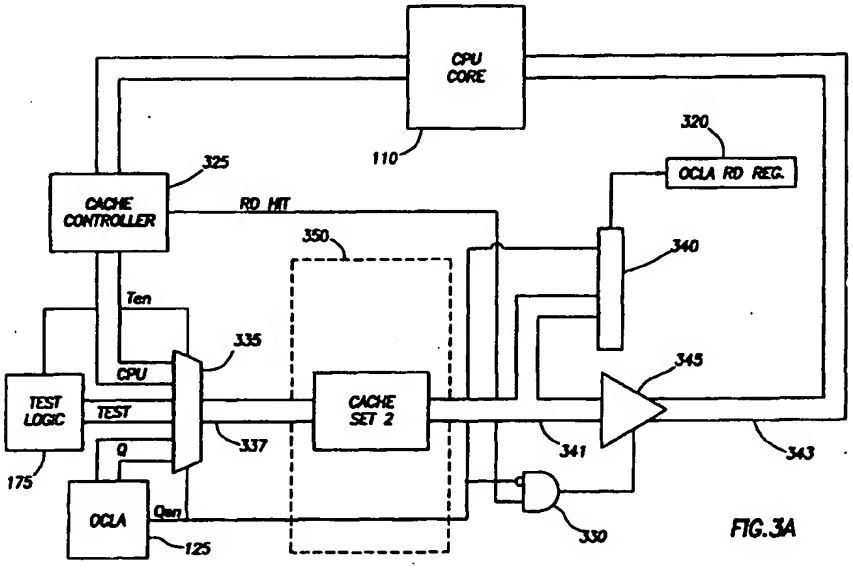

FIG. 3A

Sheet 4 of 5 – Drawings
Fig. 3B, replace with the following figure:

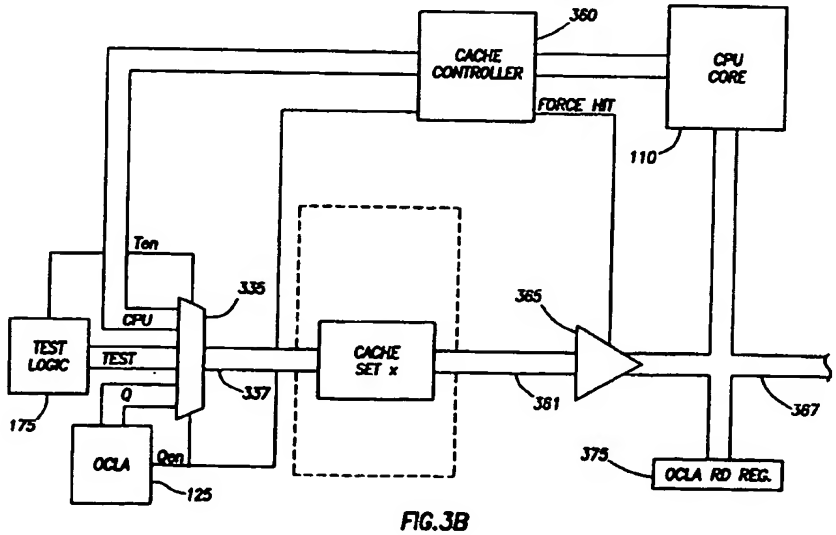

FIG. 3B

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,051,239 B2
APPLICATION NO. : 10/034717
DATED : May 23, 2006
INVENTOR(S) . : Timothe Litt

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Sheet 5 of 5 – Drawings
Fig. 4, replace with the following figure:

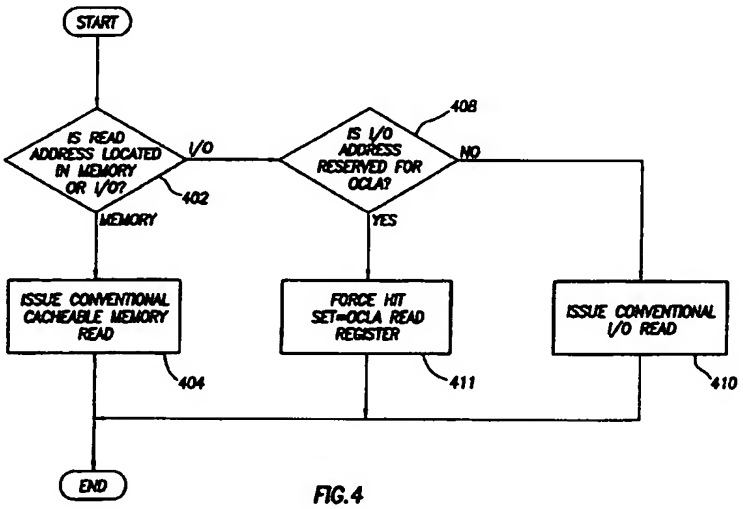

FIG. 4

Signed and Sealed this

Fifth Day of December, 2006

JON W. DUDAS
Director of the United States Patent and Trademark Office

(12) **United States Patent**
Litt

(10) **Patent No.: US 7,051,239 B2**
(45) **Date of Patent: May 23, 2006**

(54) **METHOD AND APPARATUS FOR EFFICIENTLY IMPLEMENTING TRACE AND/OR LOGIC ANALYSIS MECHANISMS ON A PROCESSOR CHIP**

(75) Inventor: **Timothe Litt**, Southborough, MA (US)

(73) Assignee: **Hewlett-Packard Development Company, L.P.**, Houston, TX (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 658 days.

(21) Appl. No.: **10/034,717**

(22) Filed: **Dec. 28, 2001**

(65) **Prior Publication Data**

US 2003/0126508 A1 Jul. 3, 2003

(51) **Int. Cl.**
G06F 11/00 (2006.01)

(52) **U.S. Cl.** **714/42**; 714/30; 714/33; 714/41

(58) **Field of Classification Search** 714/30, 714/33, 42, 41

See application file for complete search history.

(56) **References Cited**

U.S. PATENT DOCUMENTS

6,618,775	B1 *	9/2003	Davis	710/100
6,704,895	B1 *	3/2004	Swoboda et al.	714/726
6,742,145	B1 *	5/2004	Bailey et al.	714/42
6,772,369	B1 *	8/2004	Smith et al.	714/31

* cited by examiner

Primary Examiner—Scott Baderman
Assistant Examiner—Timothy M Bonura

(57) **ABSTRACT**

A system is disclosed in which an on-chip logic analyzer (OCLA) is included in an integrated circuit, such as a microprocessor. During debug modes, one or more sets of an on-chip cache memory are disabled from use by other circuitry in the integrated circuit, and reserved exclusively for use by the OCLA. Data stored in the reserved cache set can then be read out by the OCLA, and placed in a register that can be accessed by other logic internal or external to the integrated circuit. If the integrated circuit is operating under normal mode, the cache memory set can be used in conventional fashion by other circuitry with in the integrated circuit to enhance performance.

22 Claims, 5 Drawing Sheets